FAIRCHILD SEMICONDUCTOR™

April 1988
Revised January 2004

# 74F181
# 4-Bit Arithmetic Logic Unit

## General Description

The 74F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

## Features

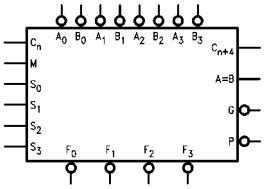
- Full lookahead for high-speed arithmetic operation on long words

## Ordering Code:

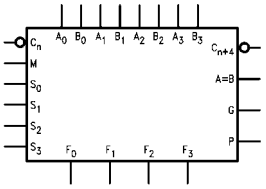
| Order Number | Package Number | Package Description |
|---|---|---|
| 74F181PC | N24A | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide |
| 74F181SPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

## Logic Symbols

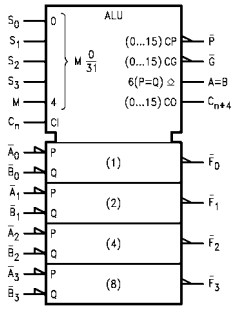
**Active-HIGH Operands**



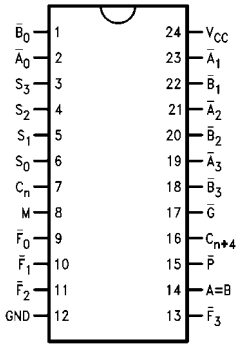

**Active-LOW Operands**




**IEEE/IEC**




## Connection Diagram



## Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
|---|---|---|---|
| $\overline{A}_0$–$\overline{A}_3$ | A Operand Inputs (Active LOW) | 1.0/3.0 | 20 μA/–1.8 mA |
| $\overline{B}_0$–$\overline{B}_3$ | B Operand Inputs (Active LOW) | 1.0/3.0 | 20 μA/–1.8 mA |
| $S_0$–$S_3$ | Function Select Inputs | 1.0/4.0 | 20 μA/–2.4 mA |
| M | Mode Control Input | 1.0/1.0 | 20 μA/–0.6 mA |
| $C_n$ | Carry Input | 1.0/5.0 | 20 μA/–3.0 mA |
| $\overline{F}_0$–$\overline{F}_3$ | Function Outputs (Active LOW) | 50/33.3 | –1 mA/20 mA |
| A = B | Comparator Output | OC (Note 1)/33.3 | (Note 1)/20 mA |
| $\overline{G}$ | Carry Generate Output (Active LOW) | 50/33.3 | –1 mA/20 mA |
| $\overline{P}$ | Carry Propagate Output (Active LOW) | 50/33.3 | –1 mA/20 mA |
| $C_{n+4}$ | Carry Output | 50/33.3 | –1 mA/20 mA |

**Note 1:** OC-Open Collector

## Functional Description

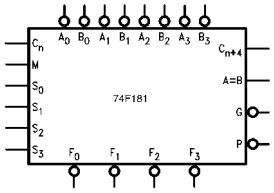
The 74F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0$–$S_3$) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $C_{n+4}$ output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the 74F181 can be used in a simple Ripple Carry mode by connecting the Carry output ($C_n$+4) signal to the Carry input ($C_n$) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 74F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

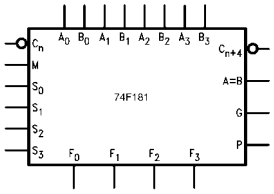
The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the $C_{n+4}$ signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

## Operation Table



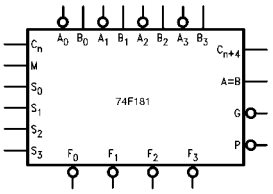
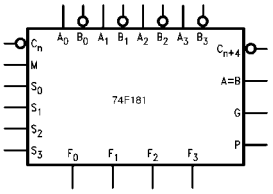

**a. All Input Data Inverted**



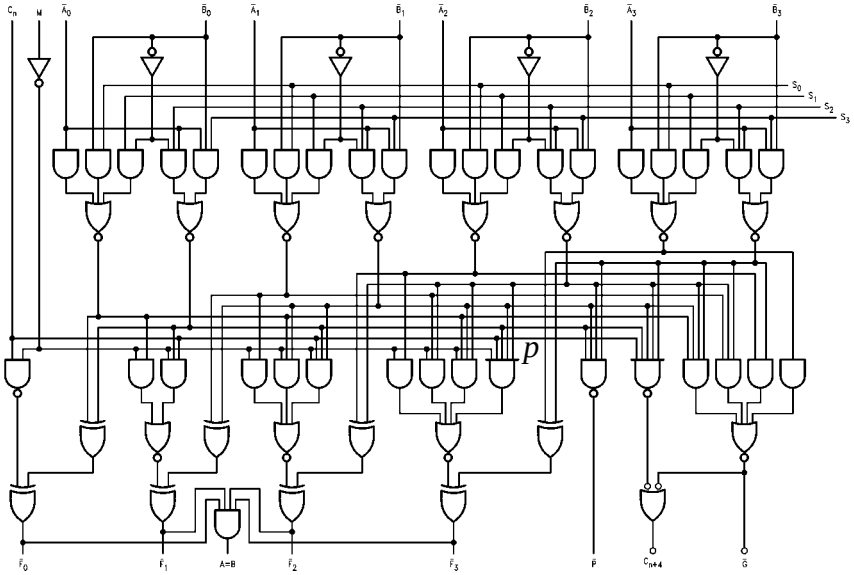

**b. All Input Data True**

| $S_0$ | $S_1$ | $S_2$ | $S_3$ | Logic (M=H) | Arithmetic (M=L, $C_0$=Inactive) | Arithmetic (M=L, $C_0$=Active) |
|---|---|---|---|---|---|---|
| L | L | L | L | $\overline{A}$ | A minus 1 | A |
| H | L | L | L | $\overline{A} \cdot \overline{B}$ | A • B minus 1 | A • B |
| L | H | L | L | $\overline{A} + B$ | A • $\overline{B}$ minus 1 | A • $\overline{B}$ |
| H | H | L | L | Logic “1” | minus 1 (2s comp.) | Zero |
| L | L | H | L | $\overline{A + B}$ | A plus (A + $\overline{B}$) | A plus (A + $\overline{B}$) plus 1 |
| H | L | H | L | $\overline{B}$ | A • B plus (A + $\overline{B}$) | A • B plus (A + $\overline{B}$) plus 1 |
| L | H | H | L | $\overline{A \oplus B}$ | A minus B minus 1 | A minus B |
| H | H | H | L | A + $\overline{B}$ | A + $\overline{B}$ | A + $\overline{B}$ plus 1 |
| L | L | L | H | $\overline{A} \cdot B$ | A plus (A + B) | A plus (A + B plus 1 |
| H | L | L | H | A⊕B | A plus B | A plus B plus 1 |
| L | H | L | H | B | A • $\overline{B}$ plus (A + B) | A • $\overline{B}$ plus (A + B) plus 1 |
| H | H | L | H | A + B | A + B | A + B plus 1 |
| L | L | H | H | Logic “0” | A plus A (2 × A) | A plus A (2 × A) plus 1 |
| H | L | H | H | A • $\overline{B}$ | A plus A • B | A plus A • B plus 1 |
| L | H | H | H | A • B | A plus A • $\overline{B}$ | A plus A • $\overline{B}$ plus 1 |
| H | H | H | H | A | A | A plus 1 |
| L | L | L | L | $\overline{A}$ | A | A plus 1 |
| H | L | L | L | $\overline{A + B}$ | A + B | A + B plus 1 |
| L | H | L | L | $\overline{A} \cdot B$ | A + $\overline{B}$ | A + $\overline{B}$ plus 1 |
| H | H | L | L | Logic “0” | minus 1 (2s comp.) | Zero |
| L | L | H | L | $\overline{A} \cdot \overline{B}$ | A plus (A • $\overline{B}$) | A plus A • $\overline{B}$ plus 1 |
| H | L | H | L | $\overline{B}$ | A • $\overline{B}$ plus (A + B) | A • B plus (A + B) plus 1 |
| L | H | H | L | A ⊕ B | A minus B minus 1 | A minus B |
| H | H | H | L | A • $\overline{B}$ | A • $\overline{B}$ minus 1 | A • $\overline{B}$ |
| L | L | L | H | $\overline{A} + B$ | A plus A • B | A plus A • B plus 1 |
| H | L | L | H | $\overline{A \oplus B}$ | A plus B | A plus B plus 1 |
| L | H | L | H | B | A • B plus (A + $\overline{B}$) | A • B plus (A + $\overline{B}$) plus 1 |
| H | H | L | H | A • B | A • B minus 1 | A • B |
| L | L | H | H | Logic “1” | A plus A (2 × A) | A plus A (2 × A) plus 1 |
| H | L | H | H | A + $\overline{B}$ | A plus (A + B) | A plus (A+B) plus 1 |
| L | H | H | H | A + B | A plus (A + $\overline{B}$) | A plus (A+$\overline{B}$) plus 1 |
| H | H | H | H | A | A minus 1 | A |

## Operation Table (Continued)

| | $S_0$ | $S_1$ | $S_2$ | $S_3$ | Logic (M=H) | Arithmetic (M=L, $C_0$=Inactive) | Arithmetic (M=L, $C_0$=Active) |
|---|---|---|---|---|---|---|---|
|   **c. A All Input Data Inverted; B Input Data True** | L | L | L | L | $\overline{A}$ | A minus 1 | A |
| | H | L | L | L | $\overline{A} + B$ | $A \bullet \overline{B}$ minus 1 | $A \bullet B$ |
| | L | H | L | L | $\overline{A} \bullet \overline{B}$ | $A \bullet B$ minus 1 | $A \bullet B$ |
| | H | H | L | L | Logic “1” | minus 1 (2s comp.) | Zero |
| | L | L | H | L | $\overline{A} \bullet B$ | A plus $(A + B)$ | A plus $(A + B)$ plus 1 |
| | H | L | H | L | B | $A \bullet \overline{B}$ plus $(A + B)$ | $A \bullet \overline{B}$ plus $(A + B)$ plus 1 |
| | L | H | H | L | $A \oplus B$ | A plus B | A plus B plus 1 |
| | H | H | H | L | $A + B$ | $A + B$ | $A + B$ plus 1 |
| | L | L | L | H | $\overline{A + B}$ | A plus $(A + \overline{B})$ | A plus $(A + \overline{B})$ plus 1 |
| | H | L | L | H | $\overline{A \oplus B}$ | A minus B minus 1 | A minus B |
| | L | H | L | H | $\overline{B}$ | $A \bullet B$ plus $(A + \overline{B})$ | $A \bullet B$ plus $(A + \overline{B})$ plus 1 |
| | H | H | L | H | $A + \overline{B}$ | $A + \overline{B}$ | $A + \overline{B}$ plus 1 |
| | L | L | H | H | Logic “0” | A plus A $(2 \times A)$ | A plus A $(2 \times A)$ plus 1 |
| | H | L | H | H | $A \bullet B$ | A plus $A \bullet \overline{B}$ | A plus $A \bullet \overline{B}$ plus 1 |
| | L | H | H | H | $A \bullet \overline{B}$ | A plus $A \bullet B$ | A plus $A \bullet B$ plus 1 |
| | H | H | H | H | A | A | A plus 1 |
|   **d. A Input Data True; B Input Date Inverted** | L | L | L | L | $\overline{A}$ | A | A plus 1 |
| | H | L | L | L | $\overline{A} \bullet B$ | $A + \overline{B}$ | $A + \overline{B}$ plus 1 |
| | L | H | L | L | $\overline{A + B}$ | $A + B$ | $A + B$ plus 1 |
| | H | H | L | L | Logic “0” | minus 1 (2s comp.) | Zero |
| | L | L | H | L | $\overline{A} + B$ | A plus $A \bullet B$ | A plus $A \bullet B$ plus 1 |
| | H | L | H | L | B | $A \bullet B$ plus $(A + \overline{B})$ | $A \bullet \overline{B}$ plus $(A + B)$ plus 1 |
| | L | H | H | L | $\overline{A \oplus B}$ | A plus B | A plus B plus 1 |
| | H | H | H | L | $A \bullet B$ | $A \bullet B$ minus 1 | $A \bullet B$ |
| | L | L | L | H | $\overline{A} \bullet \overline{B}$ | A plus $A \bullet \overline{B}$ | A plus $A \bullet B$ plus 1 |
| | H | L | L | H | $A \oplus B$ | A minus B minus 1 | A minus B |
| | L | H | L | H | $\overline{B}$ | $A \bullet \overline{B}$ plus $(A + B)$ | $A \bullet \overline{B}$ plus $(A + B)$ plus 1 |
| | H | H | L | H | $A \bullet \overline{B}$ | $A \bullet \overline{B}$ minus 1 | $A \bullet \overline{B}$ |
| | L | L | H | H | Logic “1” | A plus A $(2 \times A)$ | A plus A $(2 \times A)$ plus 1 |
| | H | L | H | H | $A + B$ | A plus $(A + \overline{B})$ | A plus $(A + \overline{B})$ plus 1 |
| | L | H | H | H | $A + \overline{B}$ | A plus $(A + B)$ | A plus $(A + B)$ plus 1 |
| | H | H | H | H | A | A minus 1 | A |

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 3) | −0.5V to +7.0V |
| Input Current (Note 3) | −30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

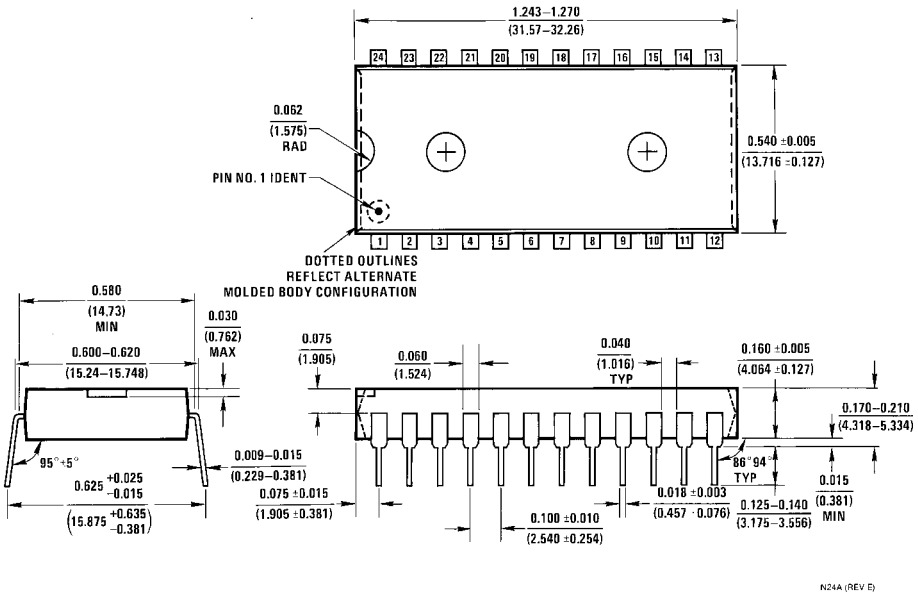
## DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH 10% $V_{CC}$ | 2.5 | | | V | Min | $I_{OH}$ = −1 mA |
| | Voltage 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −1 mA |
| $V_{OL}$ | Output LOW 10% $V_{CC}$ Voltage | | | 0.5 | V | Min | $I_{OL}$ = 20 mA |
| $I_{IH}$ | Input HIGH Current | | | 5.0 | µA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | 7.0 | µA | Max | $V_{IN}$ = 7.0V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, $C_{n+4}$) |
| $V_{ID}$ | Input Leakage Test | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA All Other Pins Grounded |
| $I_{OD}$ | Output Leakage Circuit Current | | | 3.75 | µA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{IL}$ | Input LOW Current | | | −0.6 | mA | Max | $V_{IN}$ = 0.5V (M) |
| | | | | −1.8 | | | $V_{IN}$ = 0.5V ($\overline{A}_0$, $\overline{A}_1$, $\overline{A}_3$, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_3$) |
| | | | | −2.4 | | | $V_{IN}$ = 0.5V ($S_n$, $\overline{A}_2$, $\overline{B}_2$) |
| | | | | −3.0 | | | $V_{IN}$ = 0.5V ($C_n$) |
| $I_{OS}$ | Output Short-Circuit Current | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, $C_{n+4}$) |
| $I_{OHC}$ | Open Collector, Output OFF Leakage Test | | | 250 | µA | Min | $V_O$ = $V_{CC}$ (A = B) |
| $I_{CCH}$ | Power Supply Current | | 43 | 65.0 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | 43 | 65.0 | mA | Max | $V_O$ = LOW |

## AC Electrical Characteristics

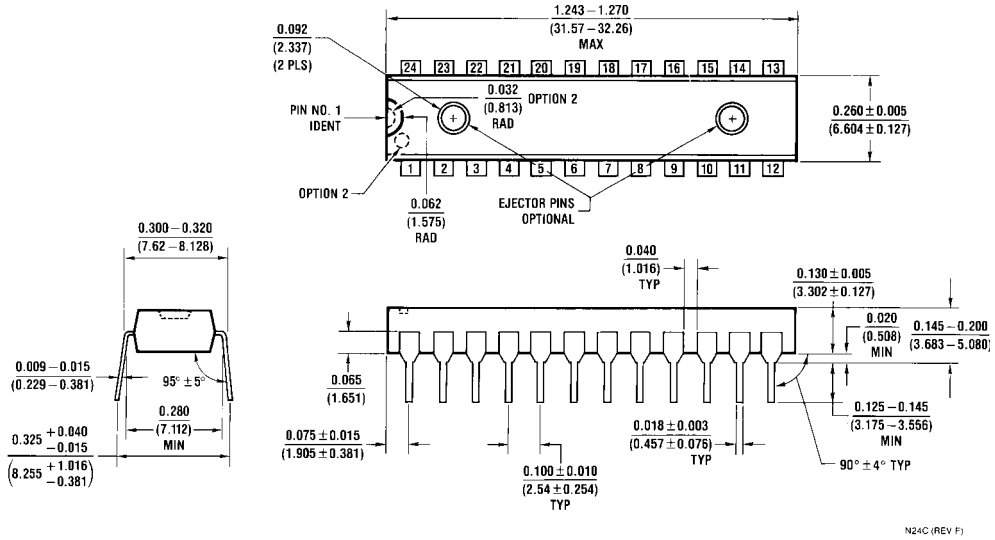
| Symbol | Parameter | | $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | $T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Path | Mode | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 6.4 | 8.5 | 3.0 | 10.0 | 3.0 | 9.5 | ns |
| $t_{PHL}$ | $C_n$ to $C_{n+4}$ | | 3.0 | 6.1 | 8.0 | 3.0 | 9.5 | 3.0 | 9.0 | |
| $t_{PLH}$ | Propagation Delay | | 5.0 | 10.0 | 13.0 | 5.0 | 15.5 | 5.0 | 14.0 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to $C_{n+4}$ | Sum | 4.0 | 9.4 | 12.0 | 3.5 | 16.5 | 4.0 | 13.0 | |
| $t_{PLH}$ | Propagation Delay | | 5.0 | 10.8 | 14.0 | 5.0 | 17.0 | 5.0 | 15.0 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to $C_{n+4}$ | Dif | 5.0 | 10.0 | 13.0 | 4.0 | 15.0 | 5.0 | 14.0 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 6.7 | 8.5 | 2.5 | 16.0 | 3.0 | 9.5 | ns |
| $t_{PHL}$ | $C_n$ to $\overline{F}$ | Any | 3.0 | 6.5 | 8.5 | 2.5 | 12.0 | 3.0 | 9.5 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 5.7 | 7.5 | 2.5 | 9.0 | 3.0 | 8.5 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ or $\overline{G}$ | Sum | 3.0 | 5.8 | 7.5 | 2.5 | 9.5 | 3.0 | 8.5 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 6.5 | 8.5 | 2.5 | 11.5 | 3.0 | 9.5 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to $\overline{G}$ | Dif | 3.0 | 7.3 | 9.5 | 2.5 | 11.0 | 3.0 | 10.5 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 5.0 | 7.0 | 2.5 | 8.5 | 3.0 | 8.0 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to $\overline{P}$ | Sum | 3.0 | 5.5 | 7.5 | 3.0 | 9.5 | 3.0 | 8.5 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 5.8 | 7.5 | 2.5 | 11.0 | 3.0 | 8.5 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to $\overline{P}$ | Dif | 4.0 | 6.5 | 8.5 | 3.0 | 11.0 | 4.0 | 9.5 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 7.0 | 9.0 | 3.0 | 14.5 | 3.0 | 10.0 | ns |
| $t_{PHL}$ | $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ | Sum | 3.0 | 7.2 | 10.0 | 3.0 | 14.5 | 3.0 | 10.0 | |
| $t_{PLH}$ | Propagation Delay | | 3.0 | 8.2 | 11.0 | 3.0 | 17.5 | 3.0 | 12.0 | ns |
| $t_{PHL}$ | $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ | Dif | 3.0 | 5.0 | 11.0 | 3.0 | 14.5 | 3.0 | 12.0 | |
| $t_{PLH}$ | Propagation Delay | | 4.0 | 8.0 | 10.5 | 3.5 | 16.5 | 4.0 | 11.5 | ns |
| $t_{PHL}$ | Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$ | Sum | 4.0 | 7.8 | 10.0 | 4.0 | 13.5 | 4.0 | 11.0 | |
| $t_{PLH}$ | Propagation Delay | | 4.5 | 9.4 | 12.0 | 3.5 | 17.5 | 4.5 | 13.0 | ns |
| $t_{PHL}$ | Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$ | Dif | 3.5 | 9.4 | 12.0 | 3.0 | 14.0 | 3.5 | 13.0 | |
| $t_{PLH}$ | Propagation Delay | | 4.0 | 6.0 | 9.0 | 3.5 | 14.5 | 4.0 | 10.0 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to $\overline{F}$ | Logic | 4.0 | 6.0 | 10.0 | 3.0 | 15.5 | 4.0 | 11.0 | |
| $t_{PLH}$ | Propagation Delay | | 11.0 | 18.5 | 27.0 | 8.0 | 35.0 | 11.0 | 29.0 | ns |
| $t_{PHL}$ | $\overline{A}$ or $\overline{B}$ to A = B | Dif | 6.0 | 9.8 | 12.5 | 5.5 | 21.0 | 6.0 | 13.5 | |

## Physical Dimensions inches (millimeters) unless otherwise noted




**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600" Wide**
**Package Number N24A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N24C**



**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**www.fairchildsemi.com**