

April 1988 Revised September 2000

74F181

4-Bit Arithmetic Logic Unit

General Description

The 74F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

Features

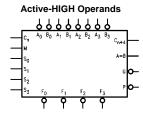
■ Full lookahead for high-speed arithmetic operation on long words

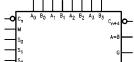
Ordering Code:

Order Number	Package Number	Package Description
74F181SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F181PC	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.600 Wide
74F181SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

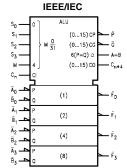
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols

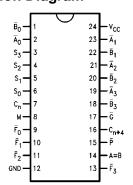




Active-LOW Operands



Connection Diagram



Unit Loading/Fan Out

Dia Nama	Description	U.L.	Input I _{IH} /I _{IL}		
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
$\overline{A}_0 - \overline{A}_3$	A Operand Inputs (Active LOW)	1.0/3.0	20 μA/–1.8 mA		
\overline{B}_0 – \overline{B}_3	B Operand Inputs (Active LOW)	1.0/3.0	20 μA/–1.8 mA		
S ₀ -S ₃	Function Select Inputs	1.0/4.0	20 μA/–2.4 mA		
М	Mode Control Input	1.0/1.0	20 μA/–0.6 mA		
C _n	Carry Input	1.0/5.0	20 μA/–3.0 mA		
\overline{F}_0 – \overline{F}_3	Function Outputs (Active LOW)	50/33.3	−1 mA/20 mA		
A = B	Comparator Output	OC (Note 1)/33.3	(Note 1)/20 mA		
G	Carry Generate Output (Active LOW)	50/33.3	−1 mA/20 mA		
P	Carry Propagate Output (Active LOW)	50/33.3	−1 mA/20 mA		
C _{n+4}	Carry Output	50/33.3	−1 mA/20 mA		

Note 1: OC-Open Collector

Functional Description

The 74F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs $(S_0\!-\!S_3)$ and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the Cn+4 output, or for carry lookahead between packages using the signals \overline{P} (Carry Propagate) and \overline{G} (Carry Generate). In the Add mode, \overline{P} indicates that \overline{F} is 15 or more. while G indicates that F is 16 or more. In the Subtract mode \overline{P} indicates that \overline{F} is zero or less, while \overline{G} indicates that \overline{F} is less than zero. \overline{P} and \overline{G} are not affected by carry in. When speed requirements are not stringent, the 74F181 can be used in a simple Ripple Carry mode by connecting the Carry output (C_n+4) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 74F181

devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four \overline{F} outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

	Operation Table							
L L L L A A B minus 1 A • B plus (A + B) A • B						Logic	Arithmetic	Arithmetic
H L L L A A B minus 1 A B plus (A B B) plus (A B B) A B plus (A B B) plus (A B B) A B plus (A B B Plus (A B B) A B plus (A B B Plus (A B B) A B plus (A B B Plus (A B B) A B plus (A B B Plus (A B B) A B plus (A B B Plus (A B B) A B plus (A B B Plus		S ₀	\mathbf{S}_{1}	S_2	S_3	(M=H)	(M=L, C ₀ =Inactive)	(M=L, C ₀ =Active)
A * B minus 1 A * B A *		L	L	L	L	Ā	A minus 1	А
H	A A B A A A B A A B A A B A A B A A B A A B A A B A A B A A B A A A B A A A B A A B A A A B A A B A A A B A A B A A A A B A A A B A A A A A B A A A A B A A A A A A A B A	Н	L	L	L	•B	A • B minus 1	A • B
2.2er0	C _n 3 7 7 7 2 2 3 3 C _{n+4}	L	Н	L	L	$\overline{A} + B$	A • B minus 1	A • B
H	→ 50	Н	Н	L	L	Logic "1"	minus 1 (2s comp.)	Zero
A · B plus (A + B) plus a A · B plus (A · B) plus a A · B plus a A · B plus (A · B) plus a A · B plus (A · B) plus a A · B plus a A ·	S ₂ 6	L	L	Н	L	$\overline{A + B}$	A plus $(A + \overline{B})$	
a. All Input Data Inverted H H H L A + B A + B A + B A + B A plus (A + B) A plus (A + B plus 1 A plus (A + B) plus (A + B) plus 1 A plus (A + B) plu		Н	L		L		' '	
L L L H A⊕B A plus (A + B) A plus (A + B plus 1 A plus B B A + B plus 1 A plus B Plus 1 A + B plus 1 A plus A • B plus 1 A + B plus 1 A • B plus (A + B) plus 1 A	<u> </u>	L	Н	Н	L			
L L L H A B A Plus (A + B) A plus 1 A plus B A plus 1 A plus B Plus 1 A Plus A	a. All Input Data Inverted	Н						· ·
L H L H B A + B plus (A + B) pl								
H H L H A+B A+B A+B A+B A+B A+B plus 1 A plus A (2 × A) plus 1 A plus A • B plus 1 A + B plus (A + B) plus 1 A + B plus 1								
L L H H L logic "0" A plus A (2 × A) A plus A (2 × A) plus 1 A plus A • B A plus A • B A plus A • B plus 1 A + B plus 1 A • B plus (A + B) A • B plus A • B plus 1 A • B plus A • B plus 1 A • B plus A • B plus 1 A • B plus A • B plus 1 A • B plus A • B plus 1 A • B plus A • B plus A • B plus 1 A • B plus A • B plu								
H L H H A A B A plus A B A plus A B A plus A B A plus A B plus 1 A B Plus A B A B Plus 1 A B Plus A B B Plus 1 A B Plus A B Plus A B Plus 1 A B Plus A B Plus A B Plus 1 A B Plus A B Plus A B Plus 1 A B Plus A B Plus A B Plus 1 A B Plus A B B Plus 1 A B Plus A B B Plus 1 A B Plus A B B Plus 1 A B Plus A B Plus 1 A B Plus A B B Plus 1 A B Plus A B B Plus 1 A B Plus A B Plus 1 A B Plus A B Plus 1 A B Plus A B Plus 1 A B Plus A B B Plus 1 A B Plus A B B Plus 1 A B Plus A B Plus B A B Plus 1 A B Plus A B B Plus 1 A B Plus A B Plus B A B Plus 1 A B Plus A B B Plus 1 A B Plus A B Plus B A B Plus B A B Plus Plus Plus Plus Plus Plus Plus Plus								
L H H H H A A B A Plus A • B A plus A • B A plus 1 A A A A A Plus 1 A A B A B A Plus 1 A B A B A Plus 1 A B A B A Plus 1 A B Plus (A + B) A Plus A • B Plus 1 A • B Plus (A + B) A Plus A • B Plus 1 A • B Plus (A + B) A Plus B A Plus A • B Plus 1 A • B Plus (A + B) A Plus B A • B Plus (A + B) A • B Plus (A + B) A Plus B A • B Plus (A + B) A • B Plus (A								1 ' ' ' '
H H H H H A A A A Plus 1 L L L L L Ā A B A A Plus 1 A B Plus (A B B) A Plus A B Plus (A B B) A Plus B Plus 1 A Plus B Plus Plus Plus Plus Plus Plus Plus Plus								·
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$								
H L L L L A B A B A B A B A B A B A B A B		1						
L H L L	1111111							
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-O C _n A ₀ B ₀ A ₁ B ₁ A ₂ B ₂ A ₃ B ₃ C							·
b. All Input Data True L L H L $\overline{A} \bullet \overline{B}$ A plus $(A \bullet \overline{B})$ A plus $(A \bullet \overline{B})$ A plus $(A + B)$ Dius $(A \bullet B)$ A plus $(A \bullet B)$ Dius $(A \bullet B)$ A plus $(A \bullet B)$ A plus $(A \bullet B)$ Dius $(A \bullet B)$ A plus $(A \bullet B)$ Dius $(A \bullet B)$ Di	M A-B							
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	S ₀ 74F181					_		
b. All Input Data True L H H L A ⊕ B A minus B minus 1 A minus B minus 1 A ⊕ B L L L L H A ⊕ B A plus A ⊕ B A plus A ⊕ B plus 1 L L L H A ⊕ B A plus B A plus B plus 1 L H L H B A ⊕ B plus (A + B) A ⊕ B plus (A + B) plus 2 H H H H H A ⊕ B A ⊕ B minus 1 A ⊕ B plus (A + B) plus 3 L L H H H A ⊕ B A plus A (2 × A) A plus A (2 × A) plus 1 H L H H H A ⊕ B A plus (A + B) A plus (A + B) plus 1 L H H H H A ⊕ B A plus (A + B) A plus (A + B) plus 1								
b. All Input Data True H H H H L L L H A • B A • B minus 1 A • B A plus A • B A plus B plus 1 A plus B plus 1 A plus B plus 1 A • B plus (A + B) A plus (A + B) <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>								
b. All Input Data True $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$								
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	b. All Input Data True							
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$								
H H L H A • B A • B minus 1 A • B L L H H H Logic "1" A plus A (2 × A) A plus A (2 × A) plus 1 H L H H A + B A plus (A + B) A plus (A + B) A plus (A + B) plus 1 L H H H A + B A plus (A + B) A plus (A + B) plus 1								· ·
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$								
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$								
L H H H A + B A plus $(A + \overline{B})$ A plus $(A + \overline{B})$ plus 1								

Operation Table (Continued)

	1				Logic	Arithmetic	Arithmetic
		•			(M=H)	(M=L, C ₀ =Inactive)	(M=L, C ₀ =Active)
	S ₀	S ₁	S ₂	S ₃	` ′		(W=L, C ₀ =Active)
Y Y Y Y	L	L	L	L	Ā	A minus 1	Α
- C ₂ A ₀ B ₀ A ₁ B ₁ A ₂ B ₂ A ₃ B ₃ C	Н	L	L	L	A + B	A • B minus 1	A • B
— M Cn+4	L	Н	L	L	Ā∙B	A • B minus 1	A • B
— S ₀ A=B —	Н	Н	L	L	Logic "1"	minus 1 (2s comp.)	Zero
s ₂ 6 0 -	L	L	Н	L	•B	A plus (A + B)	A plus (A + B) plus 1
s ₃ _{F0} _{F1} _{F2} _{F3} P	Н	L	Н	L	В	A • B plus (A + B)	$A \bullet \overline{B}$ plus $(A + B)$ plus 1
9999	L	Н	Н	L	$A \oplus B$	A plus B	A plus B plus 1
c. A All Input Data Inverted; B Input Data True	Н	Н	Н	L	A + B	A + B	A + B plus 1
o. A All input bata inverted, b input bata frue	L	L	L	Н	$\overline{A + B}$	A plus $(A + \overline{B})$	A plus $(A + \overline{B})$ plus 1
	Н	L	L	Н	Ā⊕B	A minus B minus 1	A minus B
	L	Н	L	Н	В	$A \bullet B \text{ plus } (A + \overline{B})$	A • B plus $(A + \overline{B})$ plus 1
	Н	Н	L	Н	$A + \overline{B}$	$A + \overline{B}$	$A + \overline{B}$ plus 1
	L	L	Н	Н	Logic "0"	A plus A $(2 \times A)$	A plus A $(2 \times A)$ plus 1
	Н	L	Н	Н	A • B	A plus A • B	A plus A • B plus 1
	L	Н	Н	Н	A • B	A plus A • B	A plus A • B plus 1
	Н	Н	Н	Н	Α	Α	A plus 1
1111111		L	L	L	Ā	Α	A plus 1
A _D B _D A ₁ B ₁ A ₂ B ₂ A ₃ B ₃	Н	L	L	L	Ā∙B	$A + \overline{B}$	$A + \overline{B}$ plus 1
——————————————————————————————————————		Н	L	L	A + B	A + B	A + B plus 1
S ₀ A=B 74F181	Н	Н	L	L	Logic "0"	minus 1 (2s comp.)	Zero
s₁	L	L	Н	L	$\overline{A} + B$	A plus A • B	A plus A • B plus 1
$ s_3$ s_0 s_1 s_2 s_3 p	Н	L	Н	L	В	$A \bullet B \text{ plus } (A + \overline{B})$	$A \bullet \overline{B}$ plus $(A + B)$ plus 1
	L	Н	Н	L	$\overline{A \oplus B}$	A plus B	A plus B plus 1
d. A Input Data True; B Input Date Inverted	Н	Н	Н	L	A • B	A • B minus 1	A • B
d. A input Data True, D input Date inverted	L	L	L	Н	Ā∙B	A plus A • B	A plus A • B plus 1
	Н	L	L	Н	A⊕B	A minus B minus 1	A minus B
	L	Н	L	Н	В	A • B plus (A + B)	$A \bullet \overline{B}$ plus $(A + B)$ plus 1
	Н	Н	L	Н	A • B	A • B minus 1	A • B
	L	L	Н	Н	Logic "1"	A plus A $(2 \times A)$	A plus A (2 × A) plus 1
	Н	L	Н	Н	A + B	A plus $(A + \overline{B})$	A plus $(A+\overline{B})$ plus 1
	L	Н	Н	Н	A + B	A plus (A + B)	A plus (A+B) plus 1
	Н	Н	Н	Н	Α	A minus 1	Α

Logic Diagram \vec{f}_0 \vec{f}_1 \vec{A} =B \vec{f}_2 \vec{f}_3 \vec{f}_3 \vec{p} \vec{C}_{n+4} \vec{c}_3 Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

-150°C Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$

Voltage Applied to Output in HIGH State (with V_{CC} = 0V)

 $\begin{array}{ll} \mbox{Standard Output} & -0.5\mbox{V to V}_{\mbox{CC}} \\ \mbox{3-STATE Output} & -0.5\mbox{V to } +5.5\mbox{V} \end{array}$

Current Applied to Output

Free Air Ambient Temperature $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Recommended Operating

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

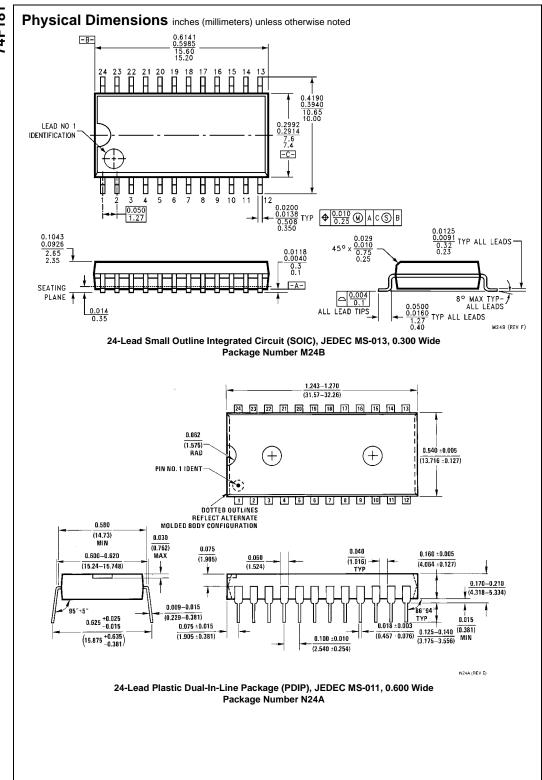
 $\textbf{Note 3:} \ \textbf{Either voltage limit or current limit is sufficient to protect inputs.}$

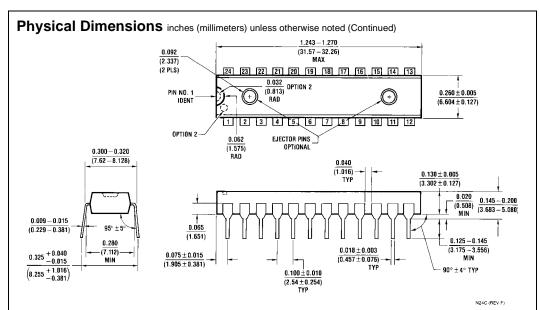
DC Electrical Characteristics

Symbol	Parameter	Min	Тур	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH 10% \	V _{CC} 2.5			V	Min	I _{OH} = -1 mA
	Voltage 5% \	V _{CC} 2.7			· ·	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW 10% \	V _{CC}		0.5	V	Min	I _{OI} = 20 mA
	Voltage				V	IVIIII	10L - 20 111A
I _{IH}	Input HIGH			5.0	μА	Max	V _{IN} = 2.7V
	Current				μΛ	IVIAX	VIN - 2.7 V
I _{BVI}	Input HIGH Current			7.0	μА	Max	V _{IN} = 7.0V
	Breakdown Test				μΛ	IVIAX	VIN - 7.0 V
I _{CEX}	Output HIGH			50		Maria	$V_{OLIT} = V_{CC}(\overline{F}_p, \overline{G}, \overline{P}, C_{p+4})$
	Leakage Current				μА	Max	$V_{OUT} = V_{CC} (F_n, G, P, C_{n+4})$
V _{ID}	Input Leakage	4.75			V	0.0	I _{ID} = 1.9 μA
	Test	4.75			V	0.0	All Other Pins Grounded
I _{OD}	Output Leakage			3.75	μА	0.0	V _{IOD} = 150 mV
	Circuit Current			3.73	μΑ	0.0	All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6			V _{IN} = 0.5V (M)
				-1.8	mA	Max	$V_{IN} = 0.5V (\overline{A}_0, \overline{A}_1, \overline{A}_3, \overline{B}_0, \overline{B}_1, \overline{B}_3)$
				-2.4	IIIA	IVIAX	$V_{IN} = 0.5V (S_n, \overline{A}_2, \overline{B}_2)$
				-3.0			$V_{IN} = 0.5V (C_n)$
Ios	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0V (\overline{F}_n, \overline{G}, \overline{P}, C_{n+4})$
I _{OHC}	Open Collector, Output			250		Min	$V_O = V_{CC} (A = B)$
	OFF Leakage Test			250	μΑ	IVIII	v0 = vCC (W = D)
I _{CCH}	Power Supply Current		43	65.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		43	65.0	mA	Max	$V_O = LOW$

AC Electrical Characteristics

			$T_A = +25^{\circ}C$		$T_A = -55^{\circ}C$	c to +125°C	T _A = 0°C	Units		
Symbol	Parameter			V _{CC} = +5.0V	,	V _{CC} =	+5.0V		V _{CC} =	
				$C_L = 50 \ pF$		$\mathbf{C_L} =$	50 pF		$\mathbf{C_L} =$	
	Path	Mode	Min	Тур	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay		3.0	6.4	8.5	3.0	10.0	3.0	9.5	ns
t _{PHL}	C_n to C_{n+4}		3.0	6.1	8.0	3.0	9.5	3.0	9.0	115
t _{PLH}	Propagation Delay		5.0	10.0	13.0	5.0	15.5	5.0	14.0	ns
t _{PHL}	\overline{A} or \overline{B} to C_{n+4}	Sum	4.0	9.4	12.0	3.5	16.5	4.0	13.0	115
t _{PLH}	Propagation Delay		5.0	10.8	14.0	5.0	17.0	5.0	15.0	no
t _{PHL}	\overline{A} or \overline{B} to C_{n+4}	Dif	5.0	10.0	13.0	4.0	15.0	5.0	14.0	ns
t _{PLH}	Propagation Delay		3.0	6.7	8.5	2.5	16.0	3.0	9.5	no
t _{PHL}	C _n to F	Any	3.0	6.5	8.5	2.5	12.0	3.0	9.5	ns
t _{PLH}	Propagation Delay		3.0	5.7	7.5	2.5	9.0	3.0	8.5	no
t _{PHL}	A or B or G	Sum	3.0	5.8	7.5	2.5	9.5	3.0	8.5	ns
t _{PLH}	Propagation Delay		3.0	6.5	8.5	2.5	11.5	3.0	9.5	
t _{PHL}	A or B to G	Dif	3.0	7.3	9.5	2.5	11.0	3.0	10.5	ns
t _{PLH}	Propagation Delay		3.0	5.0	7.0	2.5	8.5	3.0	8.0	ns
t _{PHL}	A or B to P	Sum	3.0	5.5	7.5	3.0	9.5	3.0	8.5	115
t _{PLH}	Propagation Delay		3.0	5.8	7.5	2.5	11.0	3.0	8.5	ns
t _{PHL}	A or B to P	Dif	4.0	6.5	8.5	3.0	11.0	4.0	9.5	115
t _{PLH}	Propagation Delay		3.0	7.0	9.0	3.0	14.5	3.0	10.0	
t _{PHL}	$\overline{A_i}$ or $\overline{B_i}$ to $\overline{F_i}$	Sum	3.0	7.2	10.0	3.0	14.5	3.0	10.0	ns
t _{PLH}	Propagation Delay		3.0	8.2	11.0	3.0	17.5	3.0	12.0	ns
t _{PHL}	\overline{A}_i or \overline{B}_i to \overline{F}_i	Dif	3.0	5.0	11.0	3.0	14.5	3.0	12.0	115
t _{PLH}	Propagation Delay		4.0	8.0	10.5	3.5	16.5	4.0	11.5	ns
t _{PHL}	Any A or B to Any F	Sum	4.0	7.8	10.0	4.0	13.5	4.0	11.0	115
t _{PLH}	Propagation Delay		4.5	9.4	12.0	3.5	17.5	4.5	13.0	
t _{PHL}	Any A or B to Any F	Dif	3.5	9.4	12.0	3.0	14.0	3.5	13.0	ns
t _{PLH}	Propagation Delay		4.0	6.0	9.0	3.5	14.5	4.0	10.0	ns
t _{PHL}	A or B to F	Logic	4.0	6.0	10.0	3.0	15.5	4.0	11.0	115
t _{PLH}	Propagation Delay		11.0	18.5	27.0	8.0	35.0	11.0	29.0	ns
t _{PHL}	\overline{A} or \overline{B} to $A = B$	Dif	6.0	9.8	12.5	5.5	21.0	6.0	13.5	IIS





24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com