

April 1988 Revised July 1999

74F182

Carry Lookahead Generator

General Description

The 74F182 is a high-speed carry lookahead generator. It is generally used with the 74F181 or 74F381 4-bit arithmetic logic units to provide high-speed lookahead over word lengths of more than four bits.

Features

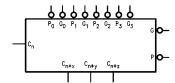
- Provides lookahead carries across a group of four ALUs
- Multi-level lookahead high-speed arithmetic operation over long word lengths

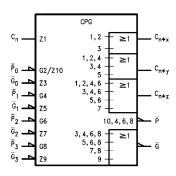
Ordering Code:

Order Number	Package Number	Package Description
74F182SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F182PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

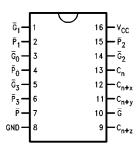
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols





Connection Diagram



Unit Loading/Fan Out

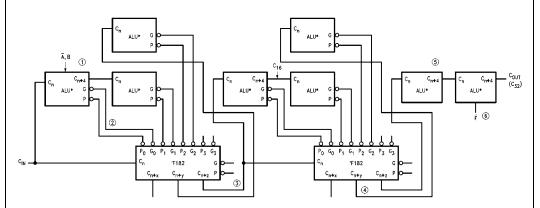
Pin Names	Description	U.L.	Input I _{IH} /I _{IL}		
Fill Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
C _n	Carry Input	1.0/2.0	20 μA/–1.2 mA		
$\overline{G}_0, \overline{G}_2$	Carry Generate Inputs (Active LOW)	1.0/14.0	20 μA/–8.4 mA		
G₁	Carry Generate Input (Active LOW)	1.0/16.0	20 μA/-9.6 mA		
\overline{G}_3	Carry Generate Input (Active LOW)	1.0/8.0	20 μA/–4.8 mA		
$\overline{P}_0, \overline{P}_1$	Carry Propagate Inputs (Active LOW)	1.0/8.0	20 μA/–4.8 mA		
\overline{P}_2	Carry Propagate Input (Active LOW)	1.0/6.0	20 μA/–3.6 mA		
P ₃	Carry Propagate Input (Active LOW)	1.0/4.0	20 μA/–2.4 mA		
$C_{n+x} - C_{n+z}$	Carry Outputs	50/33.3	−1 mA/20 mA		
G	Carry Generate Output (Active LOW)	50/33.3	−1 mA/20 mA		
P	Carry Propagate Output (Active LOW)	50/33.3	−1 mA/20 mA		

Functional Description

The 74F182 carry lookahead generator accepts up to four pairs of Active LOW Carry Propagate $(\overline{P}_0-\overline{P}_3)$ and Carry Generate $(\overline{G}_0-\overline{G}_3)$ signals and an Active HIGH Carry input (C_n) and provides anticipated Active HIGH carries $(C_{n+x},C_{n+y},C_{n+2})$ across four groups of binary adders. The 74F182 also has Active LOW Carry Propagate (\overline{P}) and Carry Generate (\overline{G}) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

Also, the 74F182 can be used with binary ALUs in an active LOW or active HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 74F181 or 74F381.

$$\begin{split} &C_{n+x} = G_0 + P_0 \, C_n \\ &C_{n+y} = G_1 + P_1 \, G_0 + P_1 \, P_0 \, C_n \\ &C_{n+z} = G_2 + P_2 \, G_1 + P_2 \, P_1 \, G_0 + P_2 \, P_1 \, P_0 \, C_n \\ &G = \overline{G}_3 + \overline{P}_3 \, \overline{G}_2 + \overline{P}_3 \, \overline{P}_2 \, \overline{G}_1 + \overline{P}_3 \, \overline{P}_2 \, \overline{P}_1 \, \overline{G}_0 \\ &P = \overline{P}_2 \, \overline{P}_2 \, \overline{P}_1 \, \overline{P}_0 \end{split}$$



*ALUs may be either 74F181 or 74F381

FIGURE 1. 32-Bit ALU with Rippled Carry between 16-Bit Lookahead ALUs

Truth Table

	Inputs									(Outputs	5	
C _n	G ₀	P ₀	G ₁	P ₁	G ₂	P ₂	G ₃	P ₃	C_{n+x}	C _{n+y}	C _{n+z}	G	P
Х	Н	Н							L				
L	Н	Χ							L				
Х	L	Χ							Н				
Н	Χ	L							Н				
Х	Х	Χ	Н	Н						L			
Х	Н	Н	Н	Χ						L			
L	Н	Χ	Н	Χ						L			
Х	Χ	Χ	L	Χ						Н			
Х	L	Χ	Χ	L						Н			
Н	Х	L	Х	L						Н			
Х	Х	Х	Х	Х	Н	Н					L		
X	X	X	H	H	Н	Х					L		
X	Н	Н	Н	Х	Н	X					L		
L	Н	Х	Н	X	Н	X					L		
X	Х	X	Х	X	L	X					Н		
×	X	X	L	X	X	L					Н		
×			X										
H	L X	X L	X	L L	X X	L L					H H		
"	^	L	^	L	^	L					п		
	Х		Х	Х	Х	Х	Н	Н				Н	
	Χ		Χ	Χ	Н	Н	Н	Χ				Н	
	Χ		Н	Н	Н	Χ	Н	Χ				Н	
	Н		Н	Χ	Н	Χ	Н	Χ				Н	
	Χ		Χ	Χ	Χ	Χ	L	Χ				L	
	Χ		Χ	Χ	L	Χ	Χ	L				L	
	Х		L	Х	Χ	L	Χ	L				L	
	L		Χ	L	Χ	L	Χ	L				L	
		Н		Χ		Χ		Χ					Н
		Χ		Н		Χ		Χ					Н
		Χ		Χ		Н		Χ					Н
		Χ		Χ		Χ		Н					Н
		L		L		L		L					L

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Logic Diagram

Absolute Maximum Ratings(Note 1)

_{150°C} Conditions

 $\begin{array}{ll} \mbox{Storage Temperature} & -65^{\circ}\mbox{C to } +150^{\circ}\mbox{C} \\ \mbox{Ambient Temperature under Bias} & -55^{\circ}\mbox{C to } +125^{\circ}\mbox{C} \\ \end{array}$

Junction Temperature under Bias -55°C to +150°C

 $\begin{array}{lll} \text{V}_{\text{CC}} \text{ Pin Potential to Ground Pin} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Voltage (Note 2)} & -0.5 \text{V to } +7.0 \text{V} \\ \text{Input Current (Note 2)} & -30 \text{ mA to } +5.0 \text{ mA} \\ \end{array}$

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

 $\begin{array}{ll} \text{Standard Output} & -0.5 \text{V to V}_{\text{CC}} \\ \text{3-STATE Output} & -0.5 \text{V to } +5.5 \text{V} \end{array}$

Current Applied to Output

 $\label{eq:lower_lower} \mbox{in LOW State (Max)} \qquad \mbox{twice the rated $I_{\rm OL}$ (mA)} \\ \mbox{ESD Last Passing Voltage (Min)} \qquad \mbox{4000V}$

Free Air Ambient Temperature $0^{\circ}\text{C} \text{ to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Recommended Operating

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

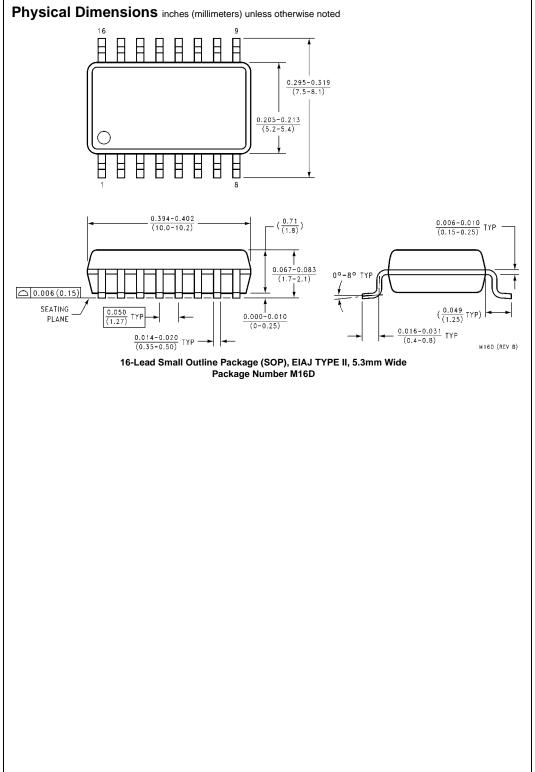
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Тур	Max	Units	v _{cc}	Conditions
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage	5% V _{CC}	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW	10% V _{CC}			0.5		Min	1 20 mA
	Voltage				0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH				5.0	μА	Max	\/ 0.7\/
	Current				5.0			$V_{IN} = 2.7V$
I _{BVI}	Input HIGH Current				7.0		Max	V 7.0V
	Breakdown Test				7.0	μΑ		V _{IN} = 7.0V
I _{CEX}	Output HIGH				50	^	Max	V V
	Leakage Current			50	μА	IVIAX	$V_{OUT} = V_{CC}$	
V _{ID}	Input Leakage	4.75			V	0.0	$I_{ID} = 1.9 \mu\text{A}$	
	Test						All Other Pins Grounded	
I _{OD}	Output Leakage			3.75	μА	0.0	$V_{IOD} = 150 \text{ mV}$	
	Circuit Current			3.75			All Other Pins Grounded	
I _{IL}	Input LOW				-1.2			$V_{IN} = 0.5V (C_n)$
	Current				-2.4			$V_{IN} = 0.5V (\overline{P}_3)$
					-3.6			$V_{IN} = 0.5V (\overline{P}_2)$
					-4.8	mA	Max	$V_{IN} = 0.5V (\overline{G}_3, \overline{P}_0, \overline{P}_1)$
					-8.4			$V_{IN} = 0.5V (\overline{G}_0, \overline{G}_2)$
					-9.6			$V_{IN} = 0.5V (\overline{G}_1)$
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current			18.4	28.0	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			23.5	36.0	mA	Max	$V_O = LOW$

AC Electrical Characteristics

		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$			$T_A = -55^{\circ}C$ to $+125^{\circ}C$ $V_{CC} = +5.0V$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$		Units	
Symbol	Parameter									
Syllibol			$\textbf{C}_{\textbf{L}} = \textbf{50 pF}$		$\mathbf{C_L} =$	50 pF	$C_L = 50 \text{ pF}$		Units	
		Min	Тур	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	3.0	6.6	8.5	3.0	12.0	3.0	9.5	ns	
t _{PHL}	C_n to C_{n+x} , C_{n+y} , C_{n+z}	3.0	6.8	9.0	3.0	11.0	3.0	10.0		
t _{PLH}	Propagation Delay	2.5	6.2	8.0	2.5	11.0	2.5	9.0		
t _{PHL}	\overline{P}_0 , \overline{P}_1 , or \overline{P}_2 to	1.5	3.7	5.0	1.0	7.0	1.5	6.0	ns	
	C _{n+x} , C _{n+y} , or C _{n+z}									
t _{PLH}	Propagation Delay	2.5	6.5	8.5	2.5	11.0	2.5	9.5		
t _{PHL}	HL \overline{G}_0 , \overline{G}_1 , or \overline{G}_2 to		3.9	5.2	1.0	7.0	1.5	6.0	ns	
	C _{n+x} , C _{n+y} , or C _{n+z}									
t _{PLH}	Propagation Delay	3.0	7.9	10.0	3.0	12.0	3.0	11.0	ns	
t _{PHL}	\overline{P}_1 , \overline{P}_2 , or \overline{P}_3 to \overline{G}	3.0	6.0	8.0	2.5	10.0	3.0	9.0		
t _{PLH}	Propagation Delay	3.0	8.3	10.5	3.0	12.0	3.0	11.5		
t _{PHL}	G _n to G	3.0	5.7	7.5	2.5	10.0	3.0	8.5	ns	
t _{PLH}	Propagation Delay	3.0	5.7	7.5	2.5	10.0	3.0	8.5	20	
t_{PHL} \overline{P}_n to \overline{P}		2.5	4.1	5.5	2.5	8.0	2.5	6.5	ns	



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.780 0.090 (18.80 - 19.81)(2.286)**16 15 14 13 12 11 10 9** 16 T5 F INDEX AREA 0.250 ± 0.010 $\overline{(6.350 \pm 0.254)}$ PIN NO. 1 PIN NO. 1 1 2 3 4 5 6 7 8 1 2 _ OPTION 01 OPTION 02 0.065 $\frac{0.130 \pm 0.005}{(3.302 \pm 0.127)}$ (1.651) $\frac{0.060}{(1.524)}$ TYP 4° TYP 0.300 - 0.320 OPTIONAL (7.620 - 8.128) 0.145 - 0.200 $\overline{(3.683 - 5.080)}$ 95°±5° $\frac{0.008 - 0.016}{(0.203 - 0.406)} \text{ TYP}$ 90° ± 4° TYP 0.020 $\frac{0.280}{(7.112)}$ MIN (0.508)0.125 - 0.150 (3.175 - 3.810) 0.030 ± 0.015 (0.762 ± 0.381) 0.014 - 0.023 0.100 ± 0.010 (0.325 +0.040 -0.015 (0.356 - 0.584) (2.540 ± 0.254) 0.050 ± 0.010 N16E (REV F) TYP (1.270 ± 0.254)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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