

Arithmetic Logic Unit

74F381

FEATURES

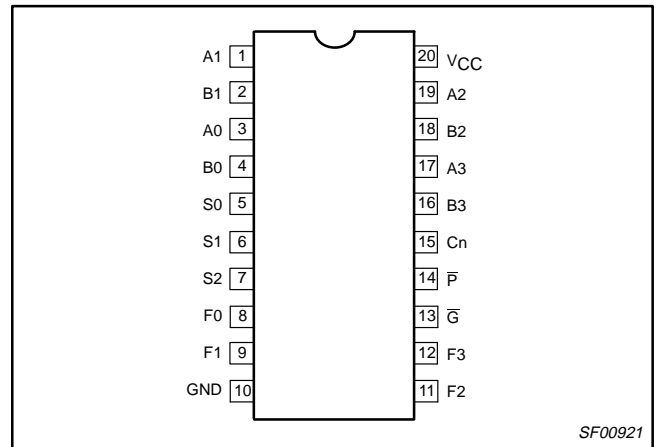
- Low-input loading minimizes drive requirements
- Performs six arithmetic and logic functions
- Selectable Low (clear) and High (preset) functions
- Carry Generate and Propagate outputs for use with Carry look-ahead generator

DESCRIPTION

The 74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Three additional Select (S0–S2) input codes force the Function outputs Low or High. Carry Propagate (\bar{P}) and Generate (\bar{G}) outputs are provided for use with the 74F182 Carry Look Ahead Generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 74F382 ALU data sheet.

Signals applied to the Select inputs (S0–S2) determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output function levels is shown in the Function Table. The circuit performs the arithmetic functions for either active-High or active-Low operands, with output levels in the same convention. In the subtract operating modes, it is necessary to force a Carry (High for active-High operands, Low for active-Low operands) into the Cn input of the least significant package. The Carry Generate (\bar{G}) and Carry Propagate (\bar{P}) outputs supply input signals to the 74F182 Carry look-ahead generator for expansion to longer word length, as shown in Figure 1. Note that a 74F382 ALU is used for the most significant package. Typical delays for Figure 1 are given in Table 1.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F381	6.5ns	59mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
20-pin plastic DIP	N74F381N
20-pin plastic SO	N74F381D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A3	A operand inputs	1.0/4.0	20 μ A/2.4mA
B0 – B3	A operand inputs	1.0/4.0	20 μ A/2.4mA
S0 – S2	Function select inputs	1.0/1.0	20 μ A/0.6mA
Cn	Carry input	1.0/4.0	20 μ A/2.4mA
\bar{P}	Carry Propagate output (active-Low)	50/33	1.0mA/20mA
\bar{G}	Carry Generate output (active-Low)	50/33	1.0mA/20mA
F0–F3	Outputs	50/33	1.0mA/20mA

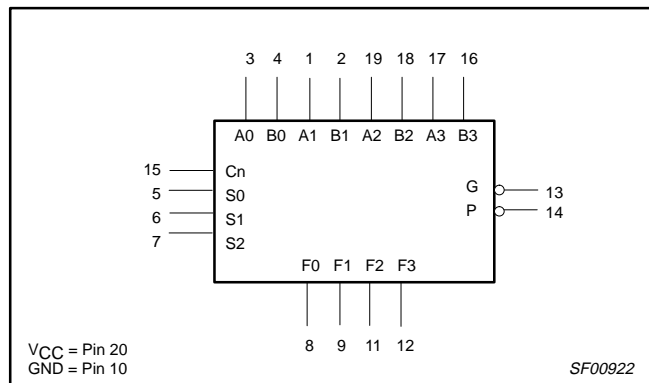
NOTE:

One (1.0) FAST unit load is defined as 20 μ A in the High state and 0.6mA in the Low state.

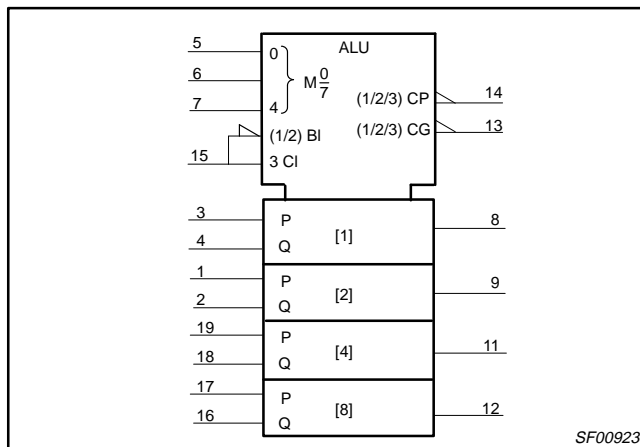
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LOGIC SYMBOL



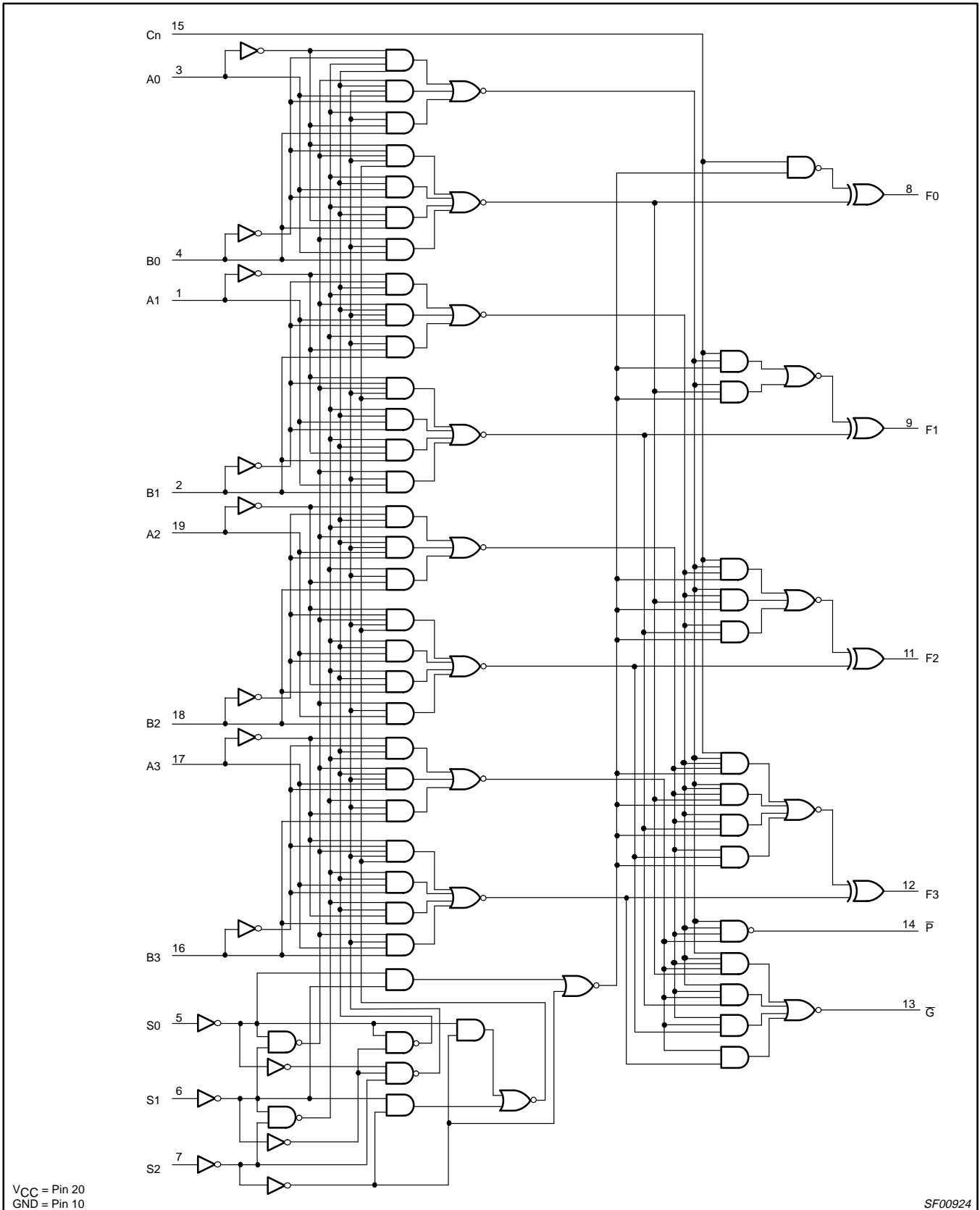
IEC/IEEE SYMBOL



Arithmetic Logic Unit

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LOGIC DIAGRAM



SF00924

Arithmetic Logic Unit

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FUNCTION TABLE

INPUTS						OUTPUTS						OPERATING MODE
S0	S1	S2	Cn	An	Bn	F0	F1	F2	F3	\bar{G}	\bar{P}	
L	L	L	X	X	X	L	L	L	L	L	L	Clear
H	L	L	L	L	L	H	H	H	H	H	L	B minus A
H	L	L	L	L	H	L	H	H	H	L	L	
H	L	L	L	H	L	L	L	L	L	H	H	
H	L	L	L	H	H	H	H	H	H	H	L	
H	L	L	H	L	L	L	L	L	L	H	L	
H	L	L	H	L	H	H	H	H	H	L	L	
H	L	L	H	H	L	H	L	L	L	H	H	
H	L	L	H	H	H	L	L	L	L	H	L	
L	H	L	L	L	L	H	H	H	H	H	L	A minus B
L	H	L	L	L	H	L	L	L	L	H	H	
L	H	L	L	H	L	L	H	H	H	L	L	
L	H	L	L	H	H	H	H	H	H	H	L	
L	H	L	H	L	L	L	L	L	L	H	L	
L	H	L	H	L	H	H	L	L	L	H	H	
L	H	L	H	H	L	H	H	H	H	L	L	
L	H	L	H	H	H	L	L	L	L	H	L	
H	H	L	L	L	L	L	L	L	L	H	H	A Plus B
H	H	L	L	L	H	H	H	H	H	H	L	
H	H	L	L	H	L	H	H	H	H	H	L	
H	H	L	L	H	H	L	H	H	H	L	L	
H	H	L	H	L	L	H	L	L	L	H	L	
H	H	L	H	L	H	L	L	L	L	H	L	
H	H	L	H	H	L	L	L	L	L	H	L	
H	H	L	H	H	H	H	H	H	H	L	L	
L	L	H	X	L	L	L	L	L	L	H	H	A ⊕ B
L	L	H	X	L	H	H	H	H	H	H	H	
L	L	H	X	H	L	H	H	H	H	H	L	
L	L	H	X	H	H	L	L	L	L	L	L	
H	L	H	X	L	L	L	L	L	L	H	H	A + B
H	L	H	X	L	H	H	H	H	H	H	H	
H	L	H	X	H	L	H	H	H	H	H	H	
H	L	H	X	H	H	H	H	H	H	H	L	
L	H	H	X	L	L	L	L	L	L	L	L	AB
L	H	H	X	L	H	L	L	L	L	H	H	
L	H	H	X	H	L	L	L	L	L	L	L	
L	H	H	X	H	H	H	H	H	H	H	L	
H	H	H	X	L	L	H	H	H	H	H	H	Preset
H	H	H	X	L	H	H	H	H	H	H	H	
H	H	H	X	H	L	H	H	H	H	H	H	
H	H	H	X	H	H	H	H	H	H	H	L	

H = High voltage level
 L = Low voltage level
 X = Don't care

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FUNCTION SELECT TABLE

SELECT			OPERATING MODE
S0	S1	S2	
L	L	L	Clear
H	L	L	B minus A
L	H	L	A minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = High voltage level
L = Low voltage level

Table 1. 16-Bit Delay Tabulation

PATH SEGMENT	TOWARD F	OUTPUT C _{n+4} , OVR
A _i or B _i to \bar{P}	7.2ns	7.2ns
\bar{P}_i to C _{n+i} (74F182)	6.2ns	6.2ns
C _n to F	8.1ns	–
C _n to C _{n+4} , OVR	–	8.0ns
Total Delay	21.5ns	21.4ns

APPLICATION

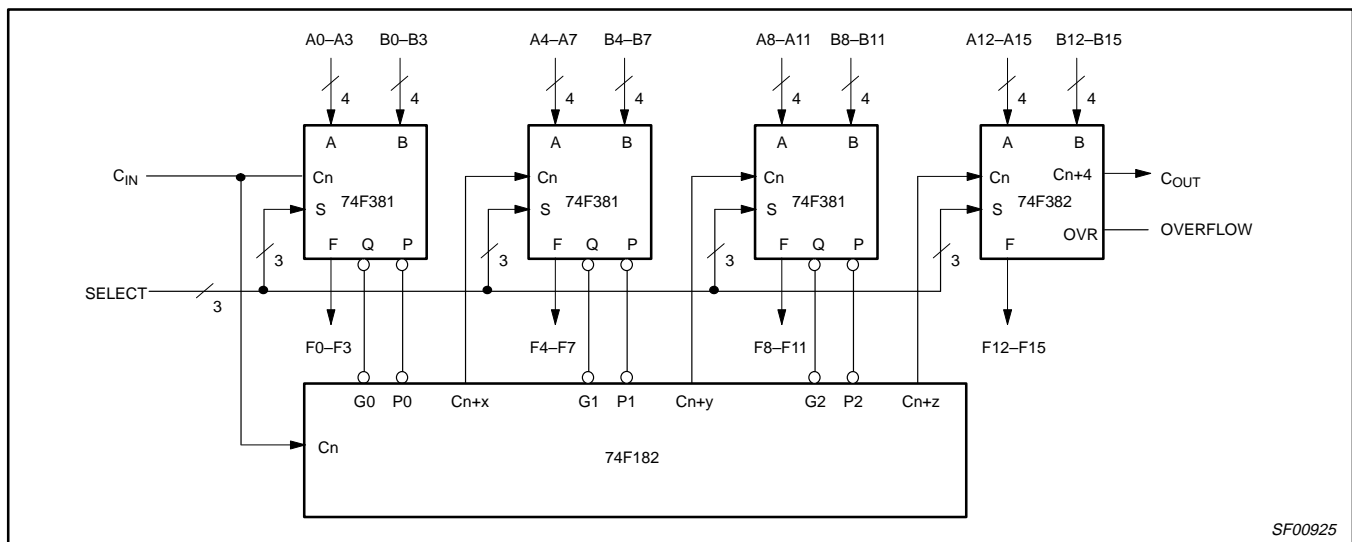


Figure 1. 16-bit Look-ahead Carry ALU Expansion

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	–0.5 to +7.0	V
V _{IN}	Input voltage	–0.5 to +7.0	V
I _{IN}	Input current	–30 to +1	mA
V _{OUT}	Voltage applied to output in High output state	–0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	40	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{STG}	Storage temperature range	–65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER SYMBOL	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-1	mA
I _{OL}	Low-level output current			20	mA
T _{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT	
				MIN	TYP ²	MAX		
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.5		V	
				±5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.30	0.50	V
				±5%V _{CC}		0.30	0.50	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current	An, Bn, Cn	V _{CC} = MAX, V _I = 0.5V				-2.4	mA
		S0, S1, S2					-0.6	mA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX		-60		-150	mA
I _{CC}	Supply current (total)		V _{CC} = MAX			59	89	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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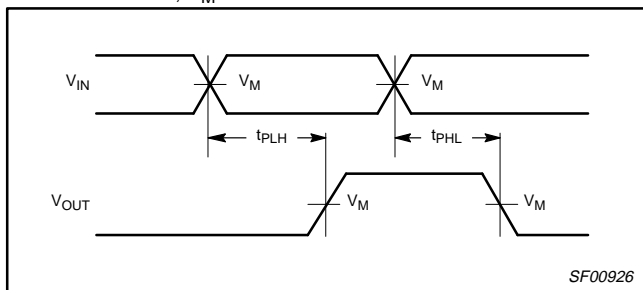
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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay C _n to F _n	Waveform 1	2.5 2.5	6.0 4.5	11.0 6.5	2.5 2.5	12.5 7.5	ns
t _{PLH} t _{PHL}	Propagation delay Any A _n or B _n to any F _n	Waveform 1	3.5 3.0	7.0 6.0	13.0 9.0	3.5 3.0	16.0 10.0	ns
t _{PLH} t _{PHL}	Propagation delay S _n to F _n	Waveform 1	5.0 4.0	9.0 7.5	20.0 10.5	5.0 4.0	21.5 11.5	ns
t _{PLH} t _{PHL}	Propagation delay A _n to B _n to \bar{G}	Waveform 1	3.5 3.0	6.5 6.0	9.0 8.5	3.5 3.0	10.0 9.0	ns
t _{PLH} t _{PHL}	Propagation delay A _n or B _n to \bar{P}	Waveform 1	3.0 3.5	5.5 6.0	8.0 8.5	3.0 3.5	9.0 9.0	ns
t _{PLH} t _{PHL}	Propagation delay S _n to \bar{G} or \bar{P}	Waveform 1	5.0 5.5	7.5 8.5	11.0 12.5	5.0 5.0	12.5 14.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for Non-Inverting or Inverting paths

TEST CIRCUIT AND WAVEFORM

Test Circuit for Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS:
 R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V _M	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006